What is claimed is:

1. A method for making a flash memory comprising:

forming a semiconductor substrate that includes a flash memory cell that has a floating gate;

forming a conductive layer on the substrate;

neutralizing process induced charge that has accumulated on the flash cell floating gate; and

forming on the conductive layer a passivation layer that is not transparent to ultraviolet light.

2. The method of claim 1 wherein process induced charge that has accumulated on the flash cell floating gate is neutralized by exposing the substrate to ultraviolet light.

3. The method of claim 2 wherein the passivation layer comprises a barrier layer and a stress reduction layer.

4. The method of claim 3 wherein the passivation layer comprises a silicon nitride layer and a polyimide layer.

5. The method of claim 4 wherein the flash cell floating gate has a gate length that is less than about 0.5 microns.

6. The method of claim 5 wherein the conductive layer forms the final metal interconnect for the flash memory, upon which is formed the passivation layer.

7. A method for making a flash memory comprising:

forming a semiconductor substrate that includes a flash memory cell that has a floating gate;

forming a conductive layer on the substrate that forms the final metal interconnect for the flash memory;

exposing the flash cell floating gate to ultraviolet light; and

forming on the conductive layer a passivation layer that is not transparent to ultraviolet light.

8. The method of claim 7 wherein the flash cell floating gate has a gate length that is less than about 0.5 microns and the passivation layer comprises a silicon nitride layer and a polyimide layer.

9. A flash memory comprising:

a semiconductor substrate that includes a flash memory cell that has a floating gate;

a conductive layer formed on the substrate; and

a passivation layer formed on the conductive layer that is not transparent to ultraviolet light.

10. The flash memory of claim 9 wherein the passivation layer comprises a barrier layer and a stress reduction layer.

11. The flash memory of claim 10 wherein the passivation layer comprises a silicon nitride layer and a polyimide layer.

12. The flash memory of claim 11 wherein the flash cell floating gate has a gate length that is less than about 0.5 microns.

13. The flash memory of claim 12 wherein the conductive layer forms the final metal interconnect for the flash memory, upon which is formed the passivation layer.

14. The flash memory of claim 13 wherein the silicon nitride layer is between about 2,000 and about 10,000 angstroms thick.

15. The flash memory of claim 9 wherein the passivation layer comprises a polyimide layer.

5